AMENDMENTS TO THE CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Previously Presented) An apparatus for etching an edge of a semiconductor wafer, comprising:

a bottom electrode, arranged below the semiconductor wafer and acting as a stage to support the semiconductor wafer;

an upper electrode, arranged above the semiconductor wafer; and

an insulating plate, arranged adjacent to the upper electrode with a gap therebetween, the insulating plate being configured such that only an edge portion of the upper electrode is exposed to the bottom electrode.

2. (Previously Presented) The apparatus of claim 1, wherein the upper electrode is

a solid plate upper electrode, arranged above the semiconductor wafer.

3. (Original) The apparatus of claim 1, further comprising:

a ring type upper electrode, arranged above the semiconductor wafer.

4. (Previously Presented) The apparatus of claim 2, further

comprising:

a lower edge electrode, arranged below the semiconductor wafer,

where the solid plate upper electrode and the lower edge electrode reciprocally generate plasma at the edge and a backside of the semiconductor wafer.

5. (Previously Presented) The apparatus of claim 3, further comprising:

a lower edge electrode, arranged below the semiconductor wafer,

where the ring type upper electrode and the lower edge electrode reciprocally generate plasma at the edge and a backside of the semiconductor wafer.

6. (Previously Presented) The apparatus of claim 4, wherein any of the bottom electrode, the solid plate upper electrode, and the lower edge electrode is a cathode or an anode.

7. (Previously Presented) The apparatus of claim 2, wherein the insulating plate is arranged adjacent to the solid plate upper electrode.

8. (Previously Presented) The apparatus of claim 3, wherein the insulating plate is arranged adjacent to the ring type upper electrode.

9. (Original) The apparatus of claim 4, further comprising:

an isolator, arranged between the bottom electrode and the lower edge electrode.

10. (Original) The apparatus of claim 7, wherein a distance between the insulating plate and the semiconductor wafer is small enough to substantially prevent plasma from being formed in a center area of the semiconductor wafer.

11. (Previously Presented) The apparatus of claim 8, wherein a distance between the insulating plate and the semiconductor wafer is small enough to substantially prevent plasma from being formed in a center area of the semiconductor wafer.

12. (Original) The apparatus of claim 7, wherein the insulating plate includes a protrusion.

13. (Previously Presented) The apparatus of claim 12, wherein the protrusion includes a sloped surface and a cliff surface, the cliff surface forming a gap with the solid plate upper electrode.

14. (Original) The apparatus of claim 12, the protrusion substantially preventing etchant gas from flowing to a center area of the semiconductor wafer.

15. (Original) The apparatus of claim 13, wherein the gap controls the size of an etched area on the semiconductor wafer.

16. (Previously Presented) The apparatus of claim 7, further comprising:

additional interchangeable insulating plates, each arrangeable adjacent to the solid plate upper electrode and each having a different size gap therebetween.

17. (Original) The apparatus of claim 1, said bottom electrode including a plurality of open grooves.

18. (Original) The apparatus of claim 17, wherein the plurality of open grooves are straight or curved.

19. (Previously Presented) The apparatus of claim 4, further comprising:

an upper edge electrode, arranged above the semiconductor wafer, where the solid plate upper electrode, the lower edge electrode and the upper edge electrode reciprocally generate plasma at the edge and the backside of the semiconductor wafer.

20. (Previously Presented) The apparatus of claim 19, wherein any of the bottom electrode, the upper edge electrode, the solid plate upper

electrode, and the lower edge electrode is a cathode or an anode.

21. (Previously Presented) The apparatus of claim 19, further comprising:

an insulating plate, arranged adjacent to the solid plate upper electrode with a gap therebetween.

22. (Original) The apparatus of claim 21, wherein a distance between the insulating plate and the semiconductor wafer is small enough to substantially prevent plasma from being formed in a center area of the semiconductor wafer.

23. (Original) The apparatus of claim 21, wherein the insulating plate includes a protrusion.

24. (Original) The apparatus of claim 23, wherein the protrusion includes a sloped surface and a cliff surface, the cliff surface forming a gap with the upper edge electrode.

25. (Original) The apparatus of claim 23, the protrusion substantially preventing etchant gas from flowing to a center area of the semiconductor wafer.

26. (Original) The apparatus of claim 24, wherein the gap controls the

size of an etched area on the semiconductor wafer.

27. (Previously Presented) The apparatus of claim 21, further comprising:

additional interchangeable insulating plates, each arrangable adjacent to the solid plate upper electrode and each having a different size gap therebetween.

28. (Currently Amended) The apparatus of claim 19 [[46]], said bottom electrode including a plurality of open grooves.

29. (Original) The apparatus of claim 28, wherein the plurality of open grooves are straight or curved.

30. (Original) The apparatus of claim 1, further comprising:

an edge bead electrode for reciprocally generating plasma at the edge and the backside of the semiconductor wafer.

31. (Previously Presented) The apparatus of claim 30, further comprising:

an insulating plate, arranged adjacent to the solid plate upper electrode with a gap therebetween.

32. (Original) The apparatus of claim 31, wherein a distance between the insulating plate and the semiconductor wafer is small enough to

substantially prevent plasma from being formed in a center area of the semiconductor wafer.

33. (Original) The apparatus of claim 32, wherein the insulating plate includes a protrusion.

34. (Original) The apparatus of claim 33, wherein the protrusion includes a sloped surface and a cliff surface, the cliff surface forming a gap with the edge bead electrode.

35. (Original) The apparatus of claim 33, the protrusion substantially preventing etchant gas from flowing to a center area of the semiconductor wafer.

36. (Original) The apparatus of claim 34, wherein the gap controls the size of an etched area on the semiconductor wafer.

37. (Previously Presented) The apparatus of claim 31, further comprising:

additional interchangeable insulating plates, each arrangeable adjacent to the solid plate upper electrode and each having a different size gap therebetween.

38. (Original) The apparatus of claim 30, said bottom electrode including a plurality of open grooves.

39. (Original) The apparatus of claim 38, wherein the plurality of open grooves are straight or curved.

40. (Withdrawn) A method of etching a semiconductor wafer, comprising:

inserting a semiconductor wafer into a chamber;

increasing a pressure in the chamber;

supply at least one etchant gas to the chamber while further increasing the pressure;

supplying power to the chamber and etching the semiconductor wafer at the edge bead or the backside of the semiconductor wafer;

discontinuing the power and the etchant gas;

venting the chamber with a venting gas; and

purging the venting gas from the chamber.

41. (Withdrawn) The method of etching a semiconductor wafer, comprising:

arranging a bottom electrode below the semiconductor wafer acting as a stage to support the semiconductor wafer;

etching the semiconductor wafer at the edge bead or the backside of the semiconductor wafer; and

maintaining a gap between the semiconductor wafer and an insulating plate from 0.2 to about 1.0 mm.

42. (Withdrawn) A method of etching a semiconductor wafer, comprising:

arranging an insulating plate, including a protrusion, above the semiconductor wafer;

etching the semiconductor wafer at the edge bead or the backside of the semiconductor wafer; and

maintaining a gap between the semiconductor wafer and the insulating plate from 0.2 to about 1.0 mm.

43. (Withdrawn) A method of etching a semiconductor wafer, comprising:

arranging a bottom electrode below the semiconductor wafer, the bottom electrode including a plurality of open grooves; and

etching the semiconductor wafer at the edge bead or the backside of the semiconductor wafer.

44. (Previously Presented) An insulating plate, comprising:

a body, made of an insulating material; and

a protrusion, including a sloped surface and a cliff surface, the protrusion protruding outwardly in a direction parallel to a radial direction of the body; wherein

the insulating plate being shaped so as to guide gas away from a center portion of a semiconductor wafer.